Digital Logic Course Example Syllabus

Week	Day	Lecture Topics	Project
1	1	Class introduction and plan	No Project First Week
	2	Electric/electronic circuits; voltage, current, & power; power supplies	
	3	Inputs and outputs, switch logic	
2	4	Diodes and transistors	Introduction to the Blackboard, Vivado, and Verilog
	5	CMOS, logic gates and ICs	
	6	Logic circuits, truth tables, representations, SOP & POS forms	
3	7	Logic equations, behavioral vs. structural, basic Verilog	Basic Digital Functions
	8	The case for minimization, overview of methods, and desired outcomes	
	9	Boolean Algebra	
4	10	K-maps	Basic Combinational Circuits
	11	K-maps (large and multiple)	
	12	K-maps and don't cares	
5	13	The use of entered variables	Combinational Blocks: Multiplexors, decoders, encoder, shifter/rotator
	14	The design process; Multiplexors and applications	
	15	Decoders and applications; Mux/Demux circuits	
6	16	Encoders; shifters	Verilog for Combinational Circuits
	14	Review	
	15	**Test 1**	
7	19	Delays and glitches	Circuit Delays and Glitches
	20	Electronic memory and basic cells	
	21	Basic cells, latches and flip-flops	
8	22	Registers and counters	Latches, Flip-flops, and Registers
	23	Counters and clock dividers, sequential circuit basics	
	24	Controlling the Seven-Segment Display	
9	25	Arithmetic circuits: ripple-carry and carry-look ahead adders	Counters, Registers, and the 7Seg Display
	26	Negative numbers, encodings, and arithmetic implications	
	27	Binary and 2's complement subtractors	
10	28	Multipliers and Comparators	Adders and Multipliers
	29	ALUs	
	30	Review	
11	31	**Test 2**	Arithmetic and Logic Unit (ALU)
	32	Sequential circuit overview and architectures	
	33	State diagrams	
12	34	Complete state diagrams, rules, and state codes	Catch up – no new lab
	35	State machine implementations	
	36	Behavioral implementation of state machines in Verilog	
13	37	Stopwatch presentation: BCD counters, controller, and partitioning	A Simple Digital System: Stopwatch
	38	Structural implementations of state machines	
	39	Reaction time monitor presentation: register files, simple filters	
14	40	Clock domains and clocking considerations	A More Involved System: Reaction Time Monitor
	41	Sampling and processing inputs	
	42	Output signal timing issues	
15	43	Review	No new lab
	44	Holiday	
	45	Holiday	